Ultra-Low Power 64 GSPS Dual Channel 0.1 - 36 GHz Transceiver with SerDes Baseband Interface

Electra-M

Features

- ADC & DAC conversion rates from 40 to 64 GSPS
- Operation in 1st Nyquist zone up to 32 GHz
- ADC & DAC directly digitize frequencies through 36 GHz
- Broad instantaneous bandwidth, up to 6.4 GHz
- Scalable decimation and interpolation from 8 to 1024
- Jariet Proprietary digital compensation optimizes spectral purity
- Dual configurable channels enable multiple architectures
- Integrated digital up & down conversion
- API provides user firmware programmability to optimize on-chip direct access to registers
- Selectable internal PLL or externally supplied sample clock provides additional flexibility
- Synchronization inputs as well as direct access to coarse and fine on-chip NCOs well aligned to phased array, MIMO and all applications where data aggregation is desired
- Full duplex, half duplex, and sleep modes supported
- High integration & performance enables elimination of several RF & Microwave analog components from system block diagram, optimizing SWaP-C and thermal generation
- JESD204B and JESD204C Serial Data Interface
- Available in a high performance organic BGA package

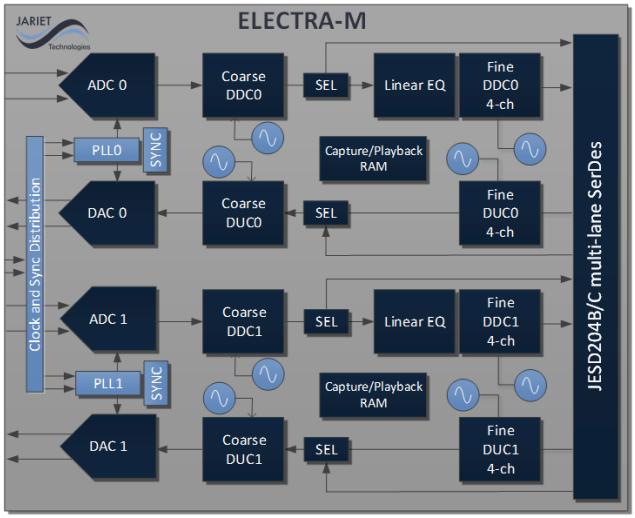
Applications

- Military & Aerospace: Radar, EW, EA, ISR, ELINT, Communications, Satellite
- Commercial: 5G Base Station, Microwave Back-haul, Test & Measurement Equipment, Radiometry, Satellite, Quantum
- Phased array antennas

General Description

The Electra-M ASIC is an ultra-high-performance, two channel ADC/DAC transceiver based on Jariet Technologies' ultra-high speed RF data converter technology. The transceiver enables the end user to eliminate substantial portions of the RF and microwave system by directly digitizing waveforms from 40 to 64 GSPS per channel with analog frequencies as high as 36 GHz and instantaneous bandwidths up to 6.4 GHz.

The 10 bit converters are extremely efficient, based on 12nm LP CMOS technology, fabricated in the United States at Global Foundries. Each channel is based on interleaved ADCs and DACs followed by programmable digital up and down conversion, linear equalization and a 16-bit SerDes baseband data interface.



Electra-M Block Diagram

25 mm x 25 mm BGA Package

A single fs/16 or fs/32 reference clock is distributed to all channels, and multiplied up by a per-channel PLL to the sample clock. The PLL can also be bypassed and an external fs/2 sample clock applied, to address phase noise sensitive applications.

The ASIC supports full synchronization capabilities, allowing alignment between channels on the ASIC and alignment of channels on multiple ASICs. A synchronization clock at fs/128, fs/256, or fs/512 is required.

Electra Family	Channels	RF (GHz)	Sample Rate (GSPS)	Min Dec/Int	Max IBW (GHz)	Tuners/ch	BGA Package	Status
Electra-MA	2T2R	0.1-36	40 to 64	8	6.4	4	25 x 25mm	Production
Electra-MK		0.1-22	40 to 58	16	2.9	2		Production
Electra-MX		0.1-12	40 to 51.2	32	1.28	2		Production
Electra-QA	4T4R	0.1-36	40 to 64	8	6.4	4	32.5 x 27.5mm	Preview
Electra-QK		0.1-22	40 to 58	16	2.9	2		Preview
Electra-QX		0.1-12	40 to 51.2	32	1.28	2		Preview